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Amendments to the Claims

This listing of claims will replace all prior versions, and listings, of the claims in the application.

All claims currently being amended are shown with deleted text struckthrough or double bracketed and new text underlined. Additionally, the status of each claim is indicated in parenthetical expression following the claim number.

Claims 1 - 8, and 11 - 26 remain.

Claims 1, 3, 5, 7, 13, 19, and 22 are being amended.

Claims 9 and 10 are being cancelled.

Claims 27 – 29 are being added.

WHAT IS CLAIMED IS:

1. (Currently Amended) A circuit comprising:

a first element sampling noise from and discharging noise to a signal line by switching a parasitic capacitance to the signal line in response to an input signal transitioning on selected edges of a clock signal; and

a second element sampling noise from and discharging noise to the signal line in response to another input signal transitioning on other edges of the clock signal differing from the selected edges of the clock signal such that a sampling and discharging frequency on the signal line is independent of the input signal and the other input signal.

2. (Original) The circuit of Claim 1, wherein the other edges of the clock signal are selected such that the sampling and discharging frequency on the signal line relates to a frequency of the clock signal.

3. (Currently Amended) The circuit of Claim 1, wherein the first element [[selectively switches a parasitic capacitance to the signal line in response to the input signal and]]

further comprises a dummy circuit switching a matching parasitic capacitance to the signal line in response to the complement of the input signal; and, wherein the second element selectively switches a parasitic capacitance to the signal line in response to the another input signal, and further comprises a dummy circuit switching another matching parasitic capacitance to the signal line in response to the complement of the another input signal.

4. (Original) The circuit of Claim 1, further comprising an operational amplifier having an input coupled to the signal line.

5. (Currently Amended) The circuit of Claim 1, wherein a selected one of [[the]] loads of the first and second elements is coupled to the signal line in response to each edge of the clock signal.

6. (Original) The circuit of Claim 1, wherein the first element comprises a data conversion element and the second element comprises a dummy data conversion element.

7. (Currently Amended) A method of reducing noise on a signal line comprising:

sampling noise from and discharging noise to a signal line by switching a parasitic capacitance to the signal line in response to an input signal transitioning on selected edges of a clock signal; and

sampling noise from and discharging noise to the signal line in response to another input signal transitioning on other edges of the clock signal differing from the selected edges of the clock signal such that a sampling and discharging frequency signal line is independent [[on the]] of the input signal and the other input signal.

8. (Original) The method of Claim 7, wherein the other edges of the clock signal are selected such that noise on the signal line relates to a frequency of the clock signal.

9. (Cancelled)

10. (Currently Amended) The method of Claim 7, wherein sampling noise from and discharging noise to the signal line in response to the another input signal comprises switching a parasitic capacitance to the signal line in response to the another input signal.

11. (Original) The method of Claim 7, wherein noise is sampled from and discharged to the signal line on every edge of the clock signal.

12. (Original) A digital to analog converter comprising:

an operational amplifier having differential inputs coupled to a pair of differential signal lines;

a data conversion element for selectively switching a signal onto a selected one of the pair of differential signal lines in response to an input signal transitioning in response to corresponding edges of a clock signal, the data conversion element having a capacitance; and

a dummy conversion element for selectively coupling a capacitance matching the capacitance of the data conversion element to a selected one of the pair of signal lines in response to an other input signal, the other input signal transitioning on other edges of the clock signal such that a sampling and discharging rate on the signal lines relates to a frequency of the clock signal.

13. (Currently Amended) The digital to analog converter of Claim 12,further comprising a dummy circuit cross-coupled to the data conversion element and having a dummy capacitance matching the capacitance of the data conversion element, the dummy circuit coupling the dummy capacitance to a selected one of the pair of signal lines in response to the complement of the input signal, ~~anda~~ and a dummy circuit cross-coupled to the dummy conversion element and having a dummy capacitance matching the capacitance of the dummy conversion element, the dummy circuit

coupling the dummy capacitance of a selected one of the signal lines in response to the complement of the other input signal.

14. (Original) The digital to analog converter of Claim 12, wherein the data conversion element comprises a current digital to analog conversion element.

15. (Original) The digital to analog converter of Claim 12, wherein the data conversion element comprises one of an array of data conversion elements and the dummy conversion element comprises one of an array of dummy conversion elements corresponding to the array of data conversion elements.

16. (Original) The digital to analog converter of Claim 12, further comprising a delta - sigma modulator providing the input signal to the data conversion element.

17. (Original) The digital to analog converter of Claim 12, wherein a selected one of the capacitance of the data conversion element and the capacitance of dummy data conversion element is coupled to the selected one of the signal lines on every edge of the clock signal.

18. (Original) The digital to analog converter of Claim 12, wherein the input signal and the complement of the input signal overlap to cause a charge transfer between the signal lines.

19. (Currently Amended) A method of controlling noise comprising:

coupling a node <u>having a parasitic capacitance</u> to a signal line in response to an input signal transitioning on selected edges of a clock signal to sample and discharge noise from and to the signal line; and

coupling a matching node to the signal line in response to another input signal transitioning on other selected edges of the clock signal to sample and discharge noise from and to the signal line such that is sampled from and discharged to the signal line at a frequency that relates to a frequency of the clock signal.

20. (Original) The method of Claim 19, wherein coupling a node to the signal line comprises coupling a data conversion element to the signal line.

21. (Original) The method of Claim 20, wherein coupling a matching node to the signal line comprises coupling another data conversion element matching the data conversion element to the signal line in response to the another input signal.

22. (Currently Amended) A shift register comprising:

a first set of shift register elements associated with a first set of parasitic capacitive loads and presenting data on a corresponding signal line in response to a first input signal; and

a second set of shift register elements associated with a second set of loads and presenting data on the signal line in response to a second input signal such that a system loading is independent of the first and second input signals.

23. (Original) The shift register of Claim 22, wherein the system loading comprises loading on a substrate.

24. (Original) The shift register of Claim 22, wherein the system loading comprises loading on a power supply.

25. (Original) A current element array controlled by a shift register, comprising:

an operational amplifier having an input coupled to a signal line;

a set of current elements each having complementary outputs; and

a set of dummy circuits selectively coupling the set of current elements to the signal line such that a load on the signal line and signal settling at the input of the operational amplifier are independent of an input signal to the current element array.

26. (Original) The current element array of Claim 25, wherein the sets of current elements and dummy circuits comprise matched sets of data conversion elements.

27. (New) The circuit of Claim 1, wherein the second element samples noise from and discharges noise to the signal line in response to the another input signal by switching another parasitic capacitance to the signal line.

28. (New) The method of Claim 19, wherein coupling a matching node to the signal line in response to another input signal comprises coupling a matching node having another parasitic capacitance to the signal line.

29. (New) The shift register of Claim 22, wherein the second set of shift register elements are associated with a second set of parasitic loads.